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FPGA BASED OFDM SYSTEM FOR WIRELESS COMMUNICATION

Prof. Rajendra V. Babar *, Miss Swati A. Jogi
*Department of Electronic and Telecommunication, Sinhgad Institute of Technology, India
Department of Electronic and Telecommunication, Sinhgad Institute of Technology, India

Keywords: OFDM, FFT, IFFT, FPGA, Xilinx, Orthogonality.

ABSTRACT
Orthogonal Frequency Division Multiplexing (OFDM) is the dominant transmission technique used in the 802.11 set of Wireless LAN standards. It divides the available spectrum into several carriers, each one modulated by a low rate. The objective is to use High-Speed-Integrated-Circuit Hardware Description Language to produce VHDL codes that carry out FFT and IFFT function. The main objective of this project is to implement the core signal processing blocks of IEEE 802.11a & IEEE 802.11b Transreceiver system on FPGA using VHDL & implement it on FPGA. Xilinx tool is used to synthesis the net list and to generate the synthesis report of our design. Modelsim is used to simulate the performance of the design at various levels it helps to generate simulation result for various data entry at various blocks in the design. The Fast Fourier Transfer and Inverse Fast Fourier Transfer have been chosen in the design instead of the DFT and IDFT because they offer good speed and less computational time. OFDM processing, which is carried out in digital domain, can be implemented as application specific integrated circuit (ASIC) or general purpose processor (GPP). General purpose processors have limitation of performances requested by wire rates. On the other side, ASIC circuits can reach high speed processing, but once they have been designed it is impossible to change them. For OFDM implementation FPGA will be the best choice since it gives flexibility to the program design besides the low cost hardware as compared to others.

INTRODUCTION
OFDM is one of the multi carrier modulation techniques. In OFDM the input data stream is separated into several parallel bit stream. Each of the bit streams is modulated at lower rates. OFDM is similar to frequency division multiplexer but much more spectrally efficient by spacing the sub-channels much closer together. This is due to special property of OFDM called as orthogonality [2]. This is done by finding frequencies that are orthogonal, which means finding frequencies that are perpendicular in a mathematical sense, allowing the spectrum of each sub-channel to overlap another without interfering with it. In figure the effect of this is seen, as the required bandwidth is greatly reduced by removing guard bands (which are present in FDM) and allowing signals to overlap.

ORTHOGONALITY
If the integral of the product of two signals is zero over a time period, then these two signals are said to be orthogonal to each other.
Therefore, orthogonality is defined by:

$$\int_0^T \cos(2\pi n f_o t)\cos(2\pi m f_o t)\,dt = 0 \qquad (n \neq m)$$

Where n and m are two unequal integers; f_ is the fundamental frequency; T is one symbol period [2].

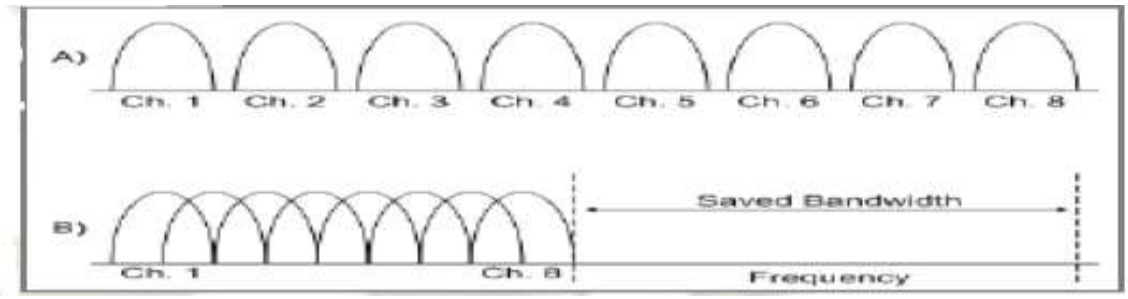

Fig 1: Bandwidth saving in OFDM

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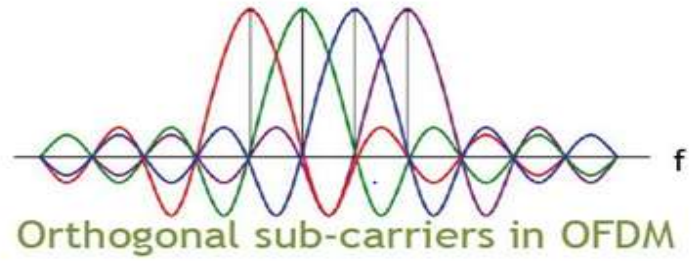

Fig 2: Orthogonality

FIELD PROGRAMMABLE GATE ARRAY

OFDM processing, which is carried out in digital domain, can be implemented as application specific integrated circuit (ASIC) or general purpose processor (GPP) [1]. GPP are at the limits of providing necessary computing performances. On the other hand, ASIC circuits can reach high speed processing, but once they have been designed it is impossible to change them. This led to development of some novel technologies such as Field programmable gate array architecture (FPGA). This platform, which is a compromise between price, speed and programmability, is very suitable for hardware implementation of OFDM system, basically because it can be easily reprogrammed with novel and improved chip designs. ASIC based designs suffer from more time to market factor, high cost and provide less flexibility. Using FPGA instead of an ASIC gives also flexibility for reconfiguration. An FPGA combines the power, density and speed characteristics of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. FPGA could be reprogrammed for new applications to meet future needs, when new design is required to fabricate. FPGA is the best choice for the OFDM implementation [5].

ADVANTAGES

The advantages of OFDM involve:

1) Bandwidth Efficiency
2) OFDM overcome the effect of ISI Eliminates ISI (Inter-Symbol Interference) and ICI (Inter-Carrier Interference)
3) Resistant to frequency selective fading.
4) Easy equalization.
5) Easy to implement.
6) Computationally efficient.

DISADVANTAGES

The disadvantages of OFDM involve:

1) High Peak to Average Power Ratio (PAPR) of transmitted signal
2) Sensitive to Doppler shift.
3) High synchronism accuracy

APPLICATIONS

The OFDM application can be seen in wired as well as wireless domain

1) Digital Audio Broadcasting (DAB).
2) Digital television DVB-T/T2 (terrestrial), DVB-H (handheld), DMB-T/H, DVB-C2 (cable).
3) Wireless LAN IEEE 802.11a, IEEE 802.11g, IEEE 802.11n, IEEE 802.11ac, and IEEE 802.11ad [6, 7].
4) WiMAX.
5) LTE and LTE Advanced mobile phone 4G standards.
6) Modern broadband and narrow power line communications.

OFDM TRANSRECEIVER

OFDM TRANSMITTER

In order to generate OFDM signal, OFDM transmitter is consisted of modules purposed for serial to parallel conversion, QAM mapping, IFFT computation. The block diagram of OFDM transmitter, showing how OFDM signal is processed on sending side. The data symbols are then parallelized with the serial to parallel conversion module in N different sub streams, where N depends on the number of points, used in the IFFT block. In our approach, we consider OFDM system with 8 subcarriers [4].

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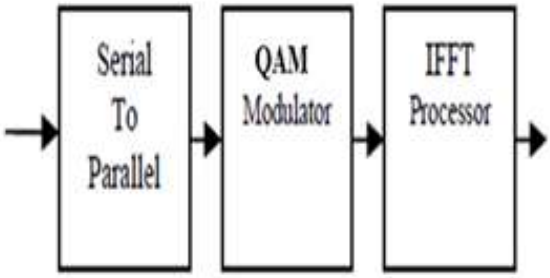

Fig 3: OFDM Transmitter.

The input data symbols are distributed to the IFFT block input, one by one, and then they are transformed from frequency to time domain symbols. Actually, each sub stream modulates a separate subcarrier through the IFFT modulation block. This block executes the computations given in equation (1), where $X(k)$ are input symbols and $x(n)$ are outputs of the IFFT block.

$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k) W_N^{-nk},\ n = 0,1,\dots,N-1,\ W_N^{-nk} = e^{\frac{j2\pi nk}{N}}$$

OFDM RECEIVER

In order to reconstruct the generated OFDM signal, OFDM receiver has to comprise modules such as FFT computation, QAM decoding and parallel to serial conversion. The block diagram of OFDM receiver, illustrating OFDM signal processing on the receiver side. The receiver performs inverse operations, in contrast to the OFDM transmitter. The input data of the OFDM receiver first goes through the serial to parallel conversion. Afterwards, the signal is passed to the 8-point FFT module, which converts it to frequency domain, and therefore retrieves the exact form of the transmitted symbols. This module executes the computations given in equation (2), where $x(n)$ are input symbols and $X(k)$ are outputs of the FFT block[3].

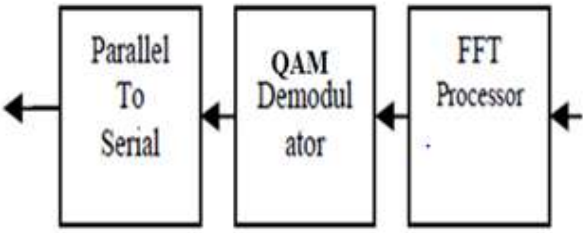

Fig 4 :OFDM Receiver.

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk},\ k = 0,1,\dots,N-1,\ W_N^{nk} = e^{\frac{-j2\pi nk}{N}}$$

The FFT block output symbols are then serially converted, with a parallel to serial conversion module. Each of the symbols is then sent to the QAM decoder that enables symbols de-mapping, according to the appropriate constellation diagram (4, 16, 64, and 256).

IMPLEMENTATION

The main implementation is of OFDM system which basically consists of transmitter & receiver section. OFDM systems rely on the IFFT for an efficient implementation of the signal modulation on the transmitter side, whereas the FFT is used for efficient demodulation of the received signal. The FFT/IFFT becomes one of the most critical modules in OFDM transceivers. In fact, the most computationally intensive parts of an OFDM system are the IFFT in the transmitter. The FFT is the second computationally intensive part in the receiver. The techniques applied to the FFT can be applied to the IFFT as well. Moreover, the IFFT can be easily obtained by manipulating the output of a FFT processor [1].HDL stands for Hardware Description Language which is used to describe any digital hardware from gates to microprocessor assembly in the form of high level programming. HDL can define any hardware at any level. Designer can use either Top-Bottom or Bottom-Up approach for hardware description. For design with increasing complexity as in our case of OFDM we generally prefer Top-Bottom approach. As seen in the block diagram the OFDM transmitter module basically consists of serial to parallel converter, QAM encoder, IFFT block & parallel to serial converter [3]. The FFT block can be implemented using shifter module, complimenter & FFT block. To find IFFT conjugate of input should be taken, then this conjugate is complimented. Next step is performing FFT operation on the complimented unit, then finally this unit is conjugated to get the IFFT. So the IFFT block can be achieved by performing several operations on the FFT block. The FFT block in the receiver section can be implemented using three modules stage1, stage2, and stage3 as we are implementing 3 stages FFT. Each stage can be implemented using two modules namely upper node & lower node. Finally each node can be implemented using adder, shifter, multiplier &complimentary modules.

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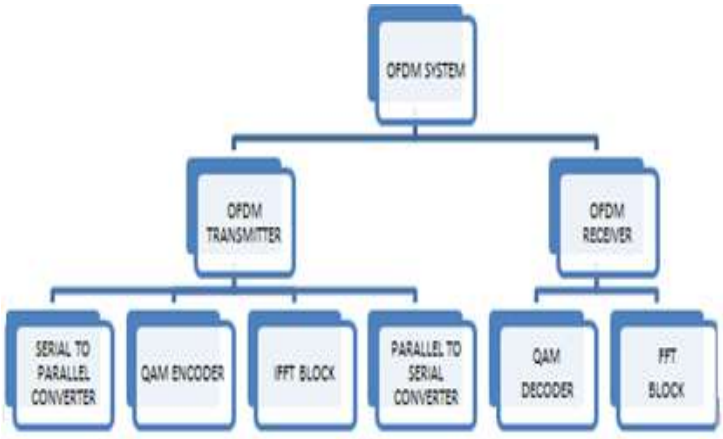

Fig 5: OFDM System

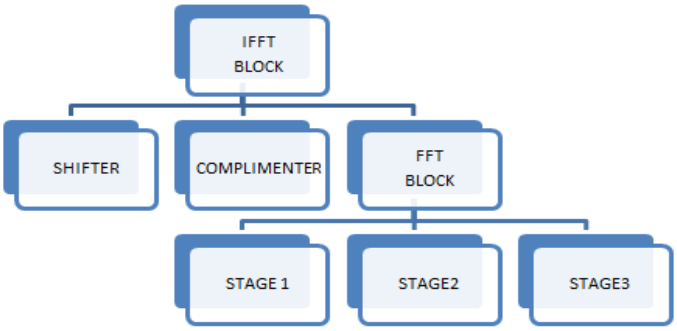

Fig 1: IFFT Block

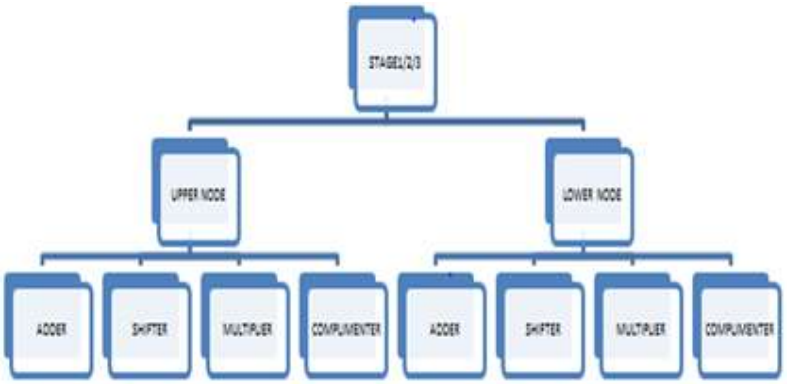

Fig 7: Stage 1/2/3

VHDL SIMULATION

The realized architectures was tested and validated the outputs are generated by a hardware simulation using Modelsim. Once the simulation results are verified next process is to perform synthesis to generate a gate level net list of the designed hardware. The realized hardware description is synthesized using Xilinx. The synthesis of OFDM system core was performed using Xilinx ISE software. Simulation is done in Modelsim and the results are as below [3].

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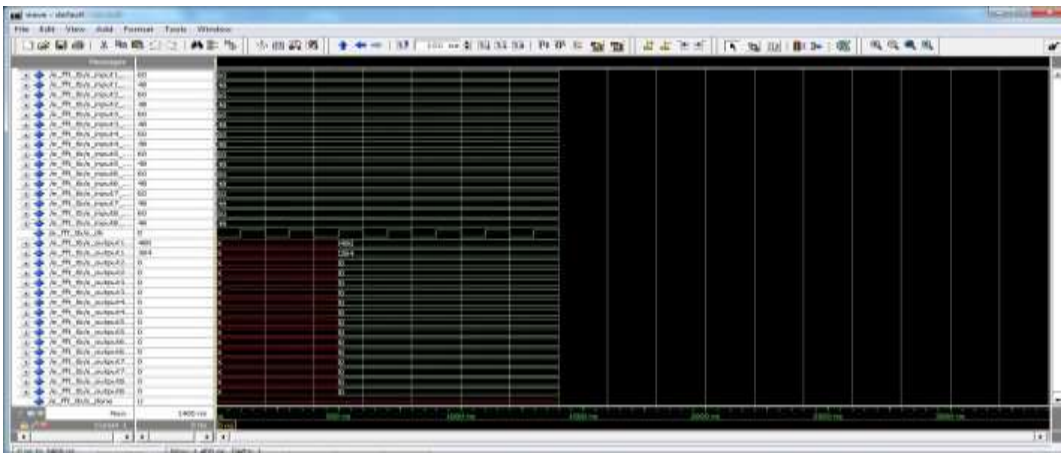

Fig 8: FFT Modelsim Output

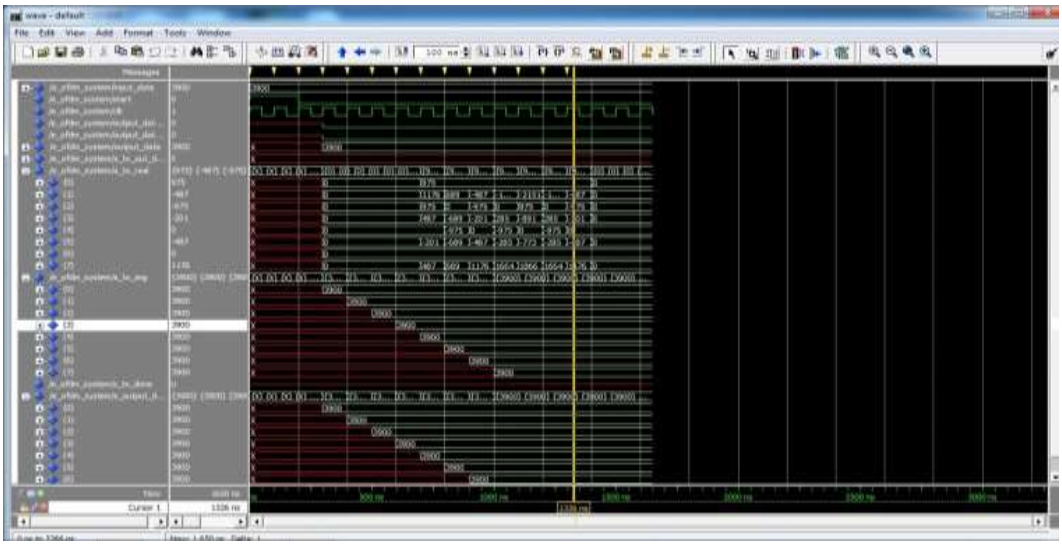

Fig 9: OFDM Modelsim Output

Fig 2: RTL schematic

CONCLUSION

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The main aim of this project is to implement the core signal processing blocks of IEEE 802.11a & IEEE 802.11b Transreciever system on FPGA using Verilog HDL to generate an optimized gate level net list which is fed to the FPGA. Xilinx tool is used to synthesis the net list and to generate the synthesis report of our design. Modelsim is used to simulate the behavior of the design at various levels it helps to generate simulation result for various data entry at various blocks in the design. FFT/IFFT is used in this work instead of DFT/IDFT because high speed and less computational time. The whole OFDM system design has been carried out using VHDL coding. Instead of structural implementation mathematical method is adopted in the design of FFT/IFFT because it is an efficient and optimized.

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